

What is claimed is:

1. A semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns,  
5 wherein each of the non-volatile memory devices has:  
a word gate formed above a semiconductor layer with a gate insulating layer interposed;  
an impurity layer formed in the semiconductor layer to form a source region or  
10 a drain region; and  
control gates in the form of side walls formed along both side surfaces of the word gate,  
wherein each of the control gates consists of a first control gate and a second control gate adjacent to each other;  
15 wherein a first insulating layer which is a stack of a first silicon oxide film, a silicon nitride film, and a second silicon oxide film is disposed between the first control gate and the semiconductor layer, and a side insulating layer is disposed between the first control gate and the word gate;  
wherein a second insulating layer which is a stack of a silicon oxide film and a  
20 silicon nitride film is disposed between the second control gate and the semiconductor layer; and  
wherein the thickness of the silicon nitride film of the second insulating layer is less than the thickness of the silicon nitride film of the first insulating layer.
- 25 2. The semiconductor device as defined in claim 1,  
wherein a charge transfer protection film is formed on the second insulating layer.

3. The semiconductor device as defined in claim 2,  
wherein the charge transfer protection film is one of a silicon oxide film and a silicon nitride oxide film.

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4. A method of manufacturing a semiconductor device having a memory region in which a memory cell array is formed of non-volatile memory devices arranged in a matrix of a plurality of rows and columns, the method comprising:

(a) forming a gate insulating layer above a semiconductor layer;

10 (b) forming a first conductive layer above the gate insulating layer;

(c) forming a stopper layer above the first conductive layer;

(d) patterning the stopper layer and the first conductive layer to form a stack of layers formed of that stopper layer and that first conductive layer;

15 (e) forming a first insulating layer by stacking a first silicon oxide film, a silicon nitride film, and a second silicon oxide film over the entire surface of the memory region;

20 (f) forming a second conductive layer above the first insulating layer, and then anisotropically etching the second conductive layer into side-wall-shaped first control gates on both side surfaces of the first conductive layer and on the semiconductor layer with the first insulating layer interposed;

(g) removing part of the second silicon oxide film of the first insulating layer and a surface portion of the silicon nitride film of the first insulating layer by using the first control gate as a mask, and defining part of the remaining first insulating layer as a second insulating layer;

25 (h) forming a third conductive layer over the entire surface of the memory region, and then anisotropically etching the third conductive layer into a second control gate on a side surface of each of the first control gates and on the semiconductor layer

with at least the second insulating layer interposed;

(i) forming an impurity layer in the semiconductor layer to form a source region or a drain region;

(j) forming a third insulating layer over the entire surface of the memory region  
5 and then removing part of the third insulating layer to expose part of the stopper layer;  
and

(k) removing the stopper layer, forming a fourth conductive layer over the entire surface of the semiconductor layer, and then patterning the fourth conductive layer to form a word line.

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5. The method of manufacturing a semiconductor device as defined in claim 4, further comprising:

forming a charge transfer protection film on the second insulating layer after forming the second insulating layer in the step (g).

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6. The method of manufacturing a semiconductor device as defined in claim 5, wherein the charge transfer protection film is one of a silicon oxide film and a silicon nitride oxide film.

20 7. The method of manufacturing a semiconductor device as defined in claim 6, wherein the charge transfer protection film is formed by a chemical vapor deposition method.

8. The method of manufacturing a semiconductor device as defined in claim 6,  
25 wherein the charge transfer protection film is formed by a thermal oxidation method.